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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,147	06/19/2003	Lawrence C. Gunn III	LUX-P004	7226

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EXAMINER	
CHIEM, DINH D	

ART UNIT	PAPER NUMBER
2883	

DATE MAILED: 09/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,147	GUNN ET AL.	
	Examiner	Art Unit	
	Erin D. Chiem	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed on June 19, 2006. Currently, claim 15 is canceled, claims 1-14 and 16-40 are pending.

Drawings

In view of the newly submitted drawings are accepted and the objection is now withdrawn.

Claim Objections

In view of the amendment to claim 32, the objection is now withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 and 16-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanguay, Jr. et al. (US Patent 5,568,574 Tanguay herein forth).

Tanguay teaches the limitation of independent claims 1 and 16 in Figure 10. The optical apparatus comprised of an array of optical grating couplers (16a, 16b) fabricated on a first

Tanguay teaches the limitation of independent claims 1 and 16 in Figure 10. The optical apparatus comprised of an array of optical grating couplers (16a, 16b) fabricated on a first substrate; and an array of optical devices (34a, 34b) on a second substrate, the first and second substrates are oriented on two separate planes that are parallel to each other; wherein the first substrate is positioned above the second substrate such that the array of optical grating couplers is optically aligned to the array of optical devices, light propagating out of the second plane from the array of optical grating couplers (see arrows) and into the first plane to the array of optical devices or out of the first plane to the array of optical devices and into the second plane to the array of optical grating couplers. The grating couplers are described as one of the 6 key features of Tanguay's invention. The diffractive elements (grating couplers) are formed on multiple hybrid silicon/GaAs substrates (col. 6, lines 44-46).

Claims 2, 5-7, 14, 17, 20-22, 29, and 30: the mechanical attachment of the two substrates may be die-attach epoxy, optical cement, or flip-chip bonding techniques (col. 8, lines 58-59). The flip-chip bonding techniques require a metallic bump, which could be lead, gold or any suitable metal, formed between two conductive pads (38), as shown in Fig. 5 element 48b. Furthermore, in the art of optoelectronic device flip-chip bonding technique is also known as Controlled Collapse Chip Connection or C4.

Claims 3 and 18: the optical devices in Figure 3 are modulators (col. 8, line 64).

Claims 4 and 19: the first substrate is a hybrid integration of silicon-based processing electronics (col. 6, lines 38-39).

Claims 8-11 and 23-26: Tanguay teaches employing electronic drive circuitry associated with each modulator element is incorporated on a substrate, and modern electronic drive circuitry

routinely uses transistors to supply electrical signals to the devices. Regarding claims 11, and 26, these are product-by-process claims and they are not given patentable weight.

Claims 12 and 27 are routine practices in the optics art when one of ordinary skill such as Tanguay would design the for the optical mode field of the grating coupler and the optical device to match such that the optical signal would couple, a fundamental concept in optical transmission.

Claims 13 and 28 are taught by Tanguay in terms of the motivation for employing parallel chip-to-chip interconnections such that chip area is reduced and allow the method allows for multiple interconnection routing on the chip and multiplex and demultiplexing of each I/O port (col. 2, lines 30-33).

Claim 31 is taught by Tanguay in Fig. 3 and 5. The optical apparatus (10) comprised of an array of optical grating couplers (16a, 16b) fabricated on a second substrate; and an array of optical devices (30a, 30b) on a first substrate, the first and second substrates are oriented on two separate planes that are parallel to each other; wherein the first substrate is positioned above the second substrate such that the array of optical grating couplers is optically aligned to the array of optical devices. Wherein the silicon-based integrated chip is mechanically fixed in optical alignment by flip-chip bonding.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 32-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanguay in view of Kamon et al. (US 5,285,258 Kamon herein forth) and Giboney et al. (US 6,318,909 B1 Giboney herein forth).

Tanguay teaches passively aligning the grating coupler array on one substrate and the optical devices array on another substrate employing mask alignment (col. 15, line 1). Although Tanguay does not explicitly teaches aligning the first element of the optical device array to the first element of the grating coupler array and on forth until the last element in both arrays are aligned, but this limitation is obviate by the end result of the alignment shown in Fig. 3-5.

However, Tanguay does not explicitly teach forming the alignment mark on the second substrate and employ vision system with pattern recognition for automated alignment. Tanguay does not explicitly teach using a plurality of mask alignment marks on a plurality of masks used to fabricate an array of optical devices for alignment.

Kamon teaches that in the actual procedure for aligning stacked wafers the process involves detecting the alignment marks, and aligning mask marks to the alignment marks, commonly these marks are gratings, which are previously formed on a semiconductor wafer at predetermined positions (col. 1, lines 16-22) for the purpose of detecting the light intensity reflected from the gratings thus determining the best alignment based on the greatest intensity light reflected from the gratings.

However, Kamon does not teach using a vision system with pattern recognition for automated alignment.

Giboney teaches pattern recognition as a method employed an automatic aligning process for optical devices and the aligning members to position (col. 13, line 67 – col. 14, line 1 – 7). Alternatively, Giboney discloses 2 other aligning methods for alignment by (1) sending optical signals to the end of the fiber optic ribbon from the alignment connector, and determine the best signal-to-noise ratio generated by the optic device while the position of the optical device is optimized (col. 14, line23 – 30). (2) Another method is send electrical signals to the transmitting elements via the electrical connector to cause the transmitting elements to generate optical signals. The optical signals at the end of the fiber optic ribbon remote from the alignment connector are monitored, and the position of the assembly relative to the device package is manipulated until the optical signals have a maximum signal-to-noise ratio, or some other indication of an optimal alignment of the assembly is obtained col. 14, line 11 – 23). Giboney's method of automated alignment is for the purpose of aligning device arrays wherein passive alignment proved to be less accurate and more labor intensive.

Since Tanguay, Kamon, and Giboney are all from the same field of endeavor, the purpose disclosed by Kamon and Giboney would have been recognized in the pertinent art of Tanguay.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to align two arrays of devices such as grating couplings and optical devices, as taught by Tanguay, to employ photolithography to alignment marks in the form of gratings onto one of the two substrate of Tanguay's device dependent on the location of the optical source and photodetector. And then to apply one of two methods taught by Giboney to detect light intensity reflected from the alignment marks to determine the best alignment based on the greatest intensity of reflected light from the alignment marks. **The motivation** for

employing automated alignment method is for its accuracy in aligning two arrays of devices and unlike passive alignment that is more labor intensive.

Claims 37-40 rejected under 35 U.S.C. 103(a) as being unpatentable over Tanguay in view of the Specification.

Tanguay teaches the flip-chip structure wherein an array of grating couplers formed on a semiconductor substrate and an array of optical devices, such as modulators and semiconductor diode lasers, formed on another semiconductor substrates and the two substrates are interconnected through flip-chip bonding. Tanguay teaches an integrated optoelectronic upper substrate to provide electronic circuitry control for any optical devices, such as the modulators and the semiconductor diode laser, and the lower substrate comprises the array of grating couplers on a planar waveguide. And Tanguay further teaches the instant interconnection provides easy coupling of the I/O ports to multiplexer and demultiplexer. Finally, in reviewing the Tanguay's reference in its entirety, Tanguay teaches how the flip-chip structure operates integrally as a device.

However, Tanguay does not explicitly teach the array of optical devices comprising photodetectors (claim 37) light splitting planar waveguide device.

The Specification, claims 3 and 18 further defines the array of optical devices is comprised of any elements from the list including VCSELs, laser, detectors, surface emitting laser, light emitting diodes, super luminescent diodes, modulators, filters, fibers, fiber components, lenses diffractive lenses, grating couplers, optical amplifiers, mirrors, or resonant cavities. The Specification, Background of the Invention, Summary of the Invention, and

Detailed Description is silent on how the flip-chip structure is critically different when employ any one of the above devices into the array of optical devices.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ any of the devices in the list above in place of the modulators and the semiconductor diode lasers, as taught by Tanguay, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70. It is respectfully noted that applicant has not disclosed any criticality in the replacement of the optical devices in the list above in applicant's Specification. It is further noted that Tanguay does not specifically limit the optical devices to be only modulators and semiconductor laser diodes. Examiner's contention of this obvious choice in design can be overcome if applicant establishes the critical and significant differences in the flip-chip structure as claimed. No new matter should be entered.

Response to Arguments

Applicant's only argument is as followed:

Tanguay alone and in combination with Kamon and/or Giboney does not disclose the device is fabricated on a first substrate comprising silicon.

This limitation has been addressed in the above rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin D. Chiem whose telephone number is (571) 272-3102. The examiner can normally be reached on Monday - Thursday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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